

SEARCH REQUEST FORM

Scientific and Technical Information Center

(75)

Requester's Full Name: David Ton Examiner #: 73667 Date: 01/23/03
Art Unit: 2133 Phone Number 306-3043 Serial Number: 09/871978
Mail Box Location: 4R17 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

Earliest Priority Filing Date: _____

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Litigation
5910181

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Searcher: <u>Shirelle Green</u>	Sequence (#) _____	<u>STN</u>
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Clerical Prep Time: _____	Patent Family _____	<u>WWW/Internet</u>
Online Time: <u>2</u>	Other _____	Other (specify) _____

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5910181

June 8, 1999

Semiconductor integrated circuit device comprising
synchronous DRAM core and logic circuit integrated into a
single chip and method of testing the synchronous DRAM core

INVENTOR: Hatakenaka, Makoto, Tokyo, JP; Yamazaki, Akira, Tokyo, JP; Tomishima, Shigeki, Tokyo, JP; Yamagata, Tadato, Tokyo, JP

APPL-NO: 964236 (08)

FILED-DATE: November 4, 1997

GRANTED-DATE: June 8, 1999

PRIORITY: April 4, 1997 - 9-086600, Japan (JP)

ASSIGNEE-AFTER-ISSUE: November 4, 1997 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., MITSUBISHI DENKI KABUSHIKI KAISHA 2- 3, MARUNOUCHI 2-CHOME, CHIYODA-KU TOKYO 1 00 JAPAN, Reel and Frame Number: 008879/0949

LEGAL-REP: Leydig, Voit & Mayer

US-MAIN-CL: 714#718

SEARCH-FLD: 371#211, 371#214, 371#216, 365#230.03, 365#230.06, 365#222, 365#236

IPC-MAIN-CL: G 06F011#0

PRIM-EXMR: Ganney, Vincent P.

ENGLISH-ABST:

A semiconductor integrated circuit device includes a logic circuit and a synchronous dynamic random access memory including a core unit, integrated on a single semiconductor chip. The semiconductor integrated circuit device includes a synchronous dynamic random access memory control circuit which receives external control signals for the synchronous dynamic random access memory from the logic circuit, and outputs internal control signals to the core unit of the synchronous dynamic random access memory. For testing of semiconductor integrated circuit device, external test signals are provided through external terminals. The external test signals are selected by a selector, and are provided to the core unit of the synchronous dynamic random access memory for testing.

LEXIS-NEXIS
Library: PATENT
File: ALL

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LEXIS-NEXIS
Library: PATENT
File: CASES

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LEXIS-NEXIS
Library: PATENT
File: JNLS

us5910181/pn

** SS 3: Results 1

Search statement 4

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1/1 PLUSPAT - (C) QUESTEL-ORBIT- image

PN - US5910181 A 19990608 [US5910181]

TI - (A) Semiconductor integrated circuit device comprising synchronous
DRAM core and logic circuit integrated into a single chip and method
of testing the synchronous DRAM core

PA - (A) MITSUBISHI ELECTRIC CORP (JP)

IN - (A) HATAKENAKA MAKOTO (JP); YAMAZAKI AKIRA (JP); TOMISHIMA SHIGEKI
(JP); YAMAGATA TADATO (JP)

AP - US96423697 19971104 [1997US-0964236]

PR - JP8660097 19970404 [1997JP-0086600]

IC - (A) G06F-011/00

EC - G11C-029/00B2B1M

- G11C-029/00B2E

PCL - ORIGINAL (O) : 714718000

DT - Corresponding document

CT - US5629898; US5761149; JP7141870

STG - (A) United States patent

AB - A semiconductor integrated circuit device includes a logic circuit and
a synchronous dynamic random access memory including a core unit,
integrated on a single semiconductor chip. The semiconductor
integrated circuit device includes a synchronous dynamic random access
memory control circuit which receives external control signals for the
synchronous dynamic random access memory from the logic circuit, and
outputs internal control signals to the core unit of the synchronous
dynamic random access memory. For testing of semiconductor integrated
circuit device, external test signals are provided through external
terminals. The external test signals are selected by a selector, and
are provided to the core unit of the synchronous dynamic random access
memory for testing.

1/1 LGST - (C) LEGSTAT

PN - US 5910181 [US5910181]

AP - US 964236/97 19971104 [1997US-0964236]

DT - US-P

ACT - 19971104 US/AE-A

APPLICATION DATA (PATENT)

{US 964236/97 19971104 [1997US-0964236]}

- 19971104 US/AS02

ASSIGNMENT OF ASSIGNOR'S INTEREST

MITSUBISHI DENKI KABUSHIKI KAISHA 2-3, MARUNOUCHI 2-CHOME, CHIYODA-KU
TOKYO 100, * HATAKENAKA, MAKOTO : 19971020; YAMAZAKI, AKIRA :

19971020; TOMISHIMA, SHIGEKI : 19971027; YAMAGATA, TADATO : 19971020

- 19990608 US/A

PATENT

UP - 2000-06

?fam us5910181/pn

1 Patent Groups
** SS 3: Results 5

Search statement 4

?famstate nonstop

1/5 INPADOC - (C) INPADOC

PN - CN 1195891 A 19981014 [CN1195891]
TI - SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING SYNCHRONOUS
DYNAMIC RANDOM MEMORY CORE
IN - HATAKENAKA MAKOTO [JP]; YAMAZAKI AKIRA [JP]; TOMISHIMA SHIGEKI [JP]
PA - MITSUBISHI ELECTRIC CORP [JP]
AP - CN 97125547/97-A 19971212 [1997CN-0125547]
PR - JP 86600/97-A 19970404 [1997JP-0086600]
IC - H01L-027/108; G01R-031/3183

2/5 INPADOC - (C) INPADOC

PN - DE 19755707 A1 19981008 [DE19755707]
TI - INTEGRIERTE HALBLEITERSCHALTUNG MIT IN EINEM EINZELCHIP INTEGRIERTEN
SYNCHRONEN DRAM-KERN UND LOGIK-SCHALTKREIS SOWIE VERFAHREN ZUM PRUEFEN
DES SYNCHRONEN DRAM-KERNS
IN - HATAKENAKA MAKOTO [JP]; TOMISHIMA SHIGEKI [JP]; YAMAZAKI AKIRA [JP];
YAMAGATA TADATO [JP]
PA - MITSUBISHI ELECTRIC CORP [JP]
AP - DE 19755707/97-A 19971215 [1997DE-1055707]
PR - JP 86600/97-A 19970404 [1997JP-0086600]
IC - G11C-011/407

1/1 LEGALI - (C) LEGSTAT

PN - DE 19755707 [DE19755707]
AP - DE 19755707/97 19971215 [1997DE-1055707]
DT - DE-P
ACTE- 19971215 DE/AE-A
DOMESTIC APPLICATION (PATENT APPLICATION)
{DE 19755707/97 19971215 [1997DE-1055707]}
- 19981008 DE/A1 [+]
LAYING OPEN FOR PUBLIC INSPECTION
- 19981008 DE/OP8 [+]
REQUEST FOR EXAMINATION AS TO PARAGRAPH 44 PATENT LAW
UP - 1999-10

3/5 INPADOC - (C) INPADOC

PN - JP 10283777 A2 19981023 [JP10283777]
TI - SEMICONDUCTOR INTEGRATED CIRCUIT WHERE SDRAM CORE AND LOGIC CIRCUIT
ARE MIXEDLY MOUNTED ON SINGLE CHIP AND TESTING METHOD OF THE SDRAM CORE
IN - HATANAKA MAKOTO; YAMAZAKI AKIRA; TOMISHIMA SHIGEKI; YAMAGATA NARIHITO
PA - MITSUBISHI ELECTRIC CORP
AP - JP 86600/97-A 19970404 [1997JP-0086600]
PR - JP 86600/97-A 19970404 [1997JP-0086600]
IC - G11C-011/407; G11C-011/401; G11C-029/00

4/5 INPADOC - (C) INPADOC

PN - TW 439036 B 20010607 [TW-439036]
TI - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE COMPRISING SYNCHRONOUS DRAM
CORE AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND METHOD OF
TESTING THE SYNCHRONOUS DRAM CORE

IN - HATAKENAKA MAKOTO [JP]; YAMAZAKI AKIRA [JP]; TOMISHIMA SHIGEKI [JP];
YAMAGATA TADATO [JP]
PA - MITSUBISHI ELECTRIC CORP [JP]
AP - TW 86117429/97-A 19971121 [1997TW-0117429]
PR - JP 86600/97-A 19970404 [1997JP-0086600]
IC - G06F-015/16

5/5 INPADOC - (C) INPADOC

PN - US 5910181 A 19990608 [US5910181]
TI - SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE COMPRISING SYNCHRONOUS DRAM
CORE AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND METHOD OF
TESTING THE SYNCHRONOUS DRAM CORE
IN - HATAKENAKA MAKOTO [JP]; YAMAZAKI AKIRA [JP]; TOMISHIMA SHIGEKI [JP];
YAMAGATA TADATO [JP]
PA - MITSUBISHI ELECTRIC CORP [JP]
AP - US 964236/97-A 19971104 [1997US-0964236]
PR - JP 86600/97-A 19970404 [1997JP-0086600]
IC - G06F-011/00

1/1 LEGALI - (C) LEGSTAT

PN - US 5910181 [US5910181]
AP - US 964236/97 19971104 [1997US-0964236]
DT - US-P
ACTE- 19971104 US/AE-A
APPLICATION DATA (PATENT)
{US 964236/97 19971104 [1997US-0964236]}
- 19971104 US/AS02
ASSIGNMENT OF ASSIGNOR'S INTEREST
MITSUBISHI DENKI KABUSHIKI KAISHA 2-3, MARUNOUCHI 2-CHOME, CHIYODA-KU
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19971020; TOMISHIMA, SHIGEKI : 19971027; YAMAGATA, TADATO : 19971020
- 19990608 US/A
PATENT
UP - 2000-06